

Figure 2

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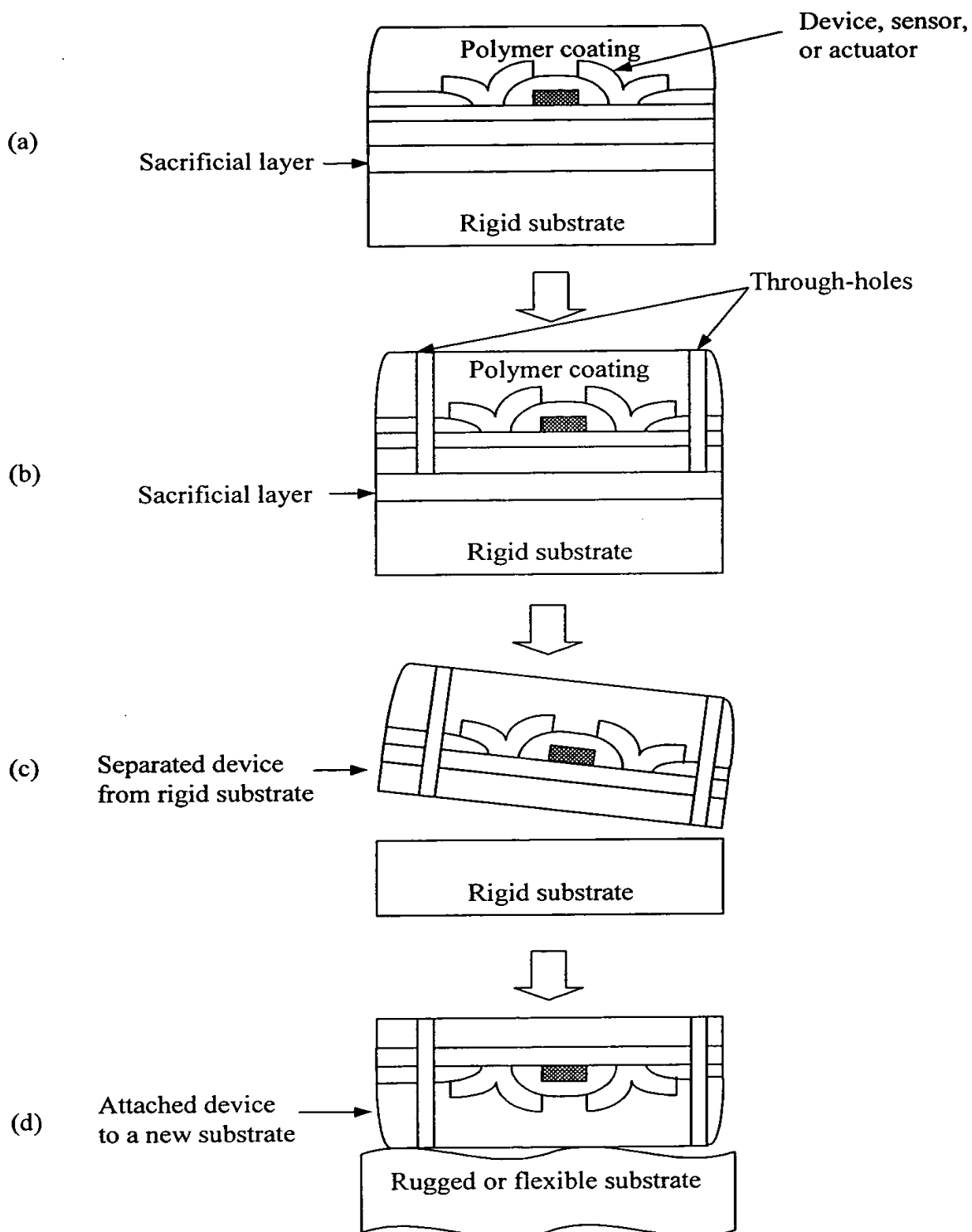


Figure 3

Figure 3

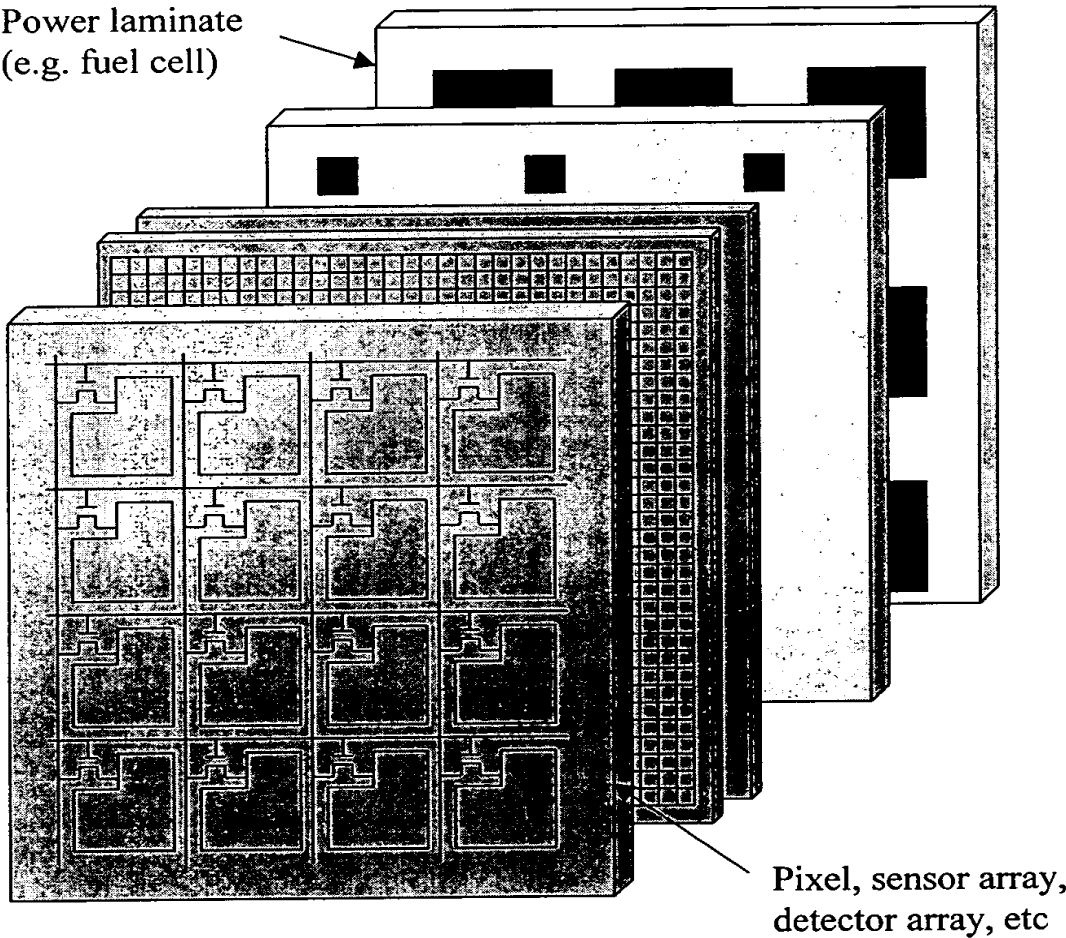


Figure 4

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(a) Sacrificial layer deposition



(b) Lithography and etching



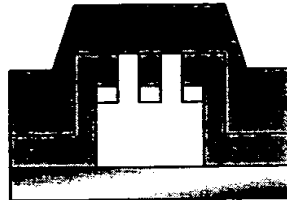
(c) Wall /capping layer deposition



(d) Wet etchant access window etching
(Holes occur as needed in top or sides for effective etching)



(e) Sacrificial layer etching



(f) Window filling



Substrate



Air (empty space)



Column/void silicon



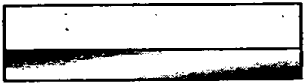
Cap layer



Wall material

Figure 5

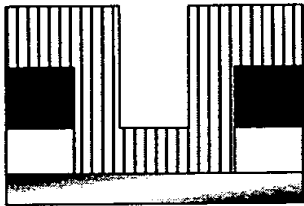
Figure 5



(a) Base layer deposition



(b) Lithography and base layer etching



(c) Sacrificial layer deposition



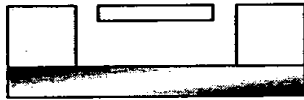
(d) Lift-off



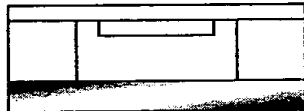
(e) Capping layer deposition



(f) Wet etchant access window etching
(Holes occur as needed in top or sides for effective etching)



(g) Sacrificial layer etching



(h) Window filling



Substrate



Air (empty space)



Column/void silicon



Stencil layer

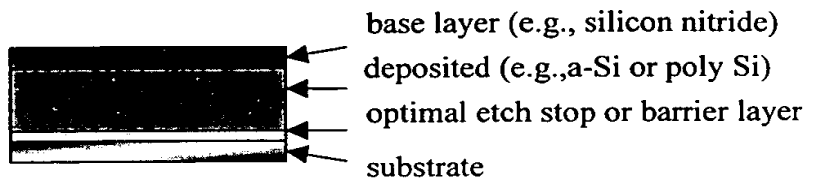


Base/wall/cap material or materials

Figure 6

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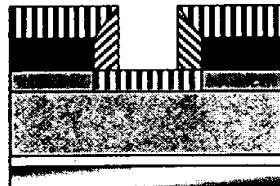
(a) Base layer deposition



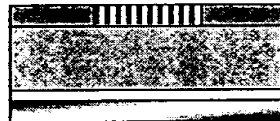
(b) Lithography and
base layer etching



(c) Sacrificial layer
deposition



(d) Lift-off



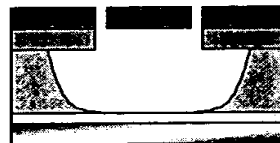
(e) Capping layer deposition



(f) Etchant access window
etching



(g) Sacrificial layer etching
and trench creation



(h) Window filling

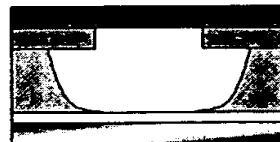


Figure 7

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05336449 041701

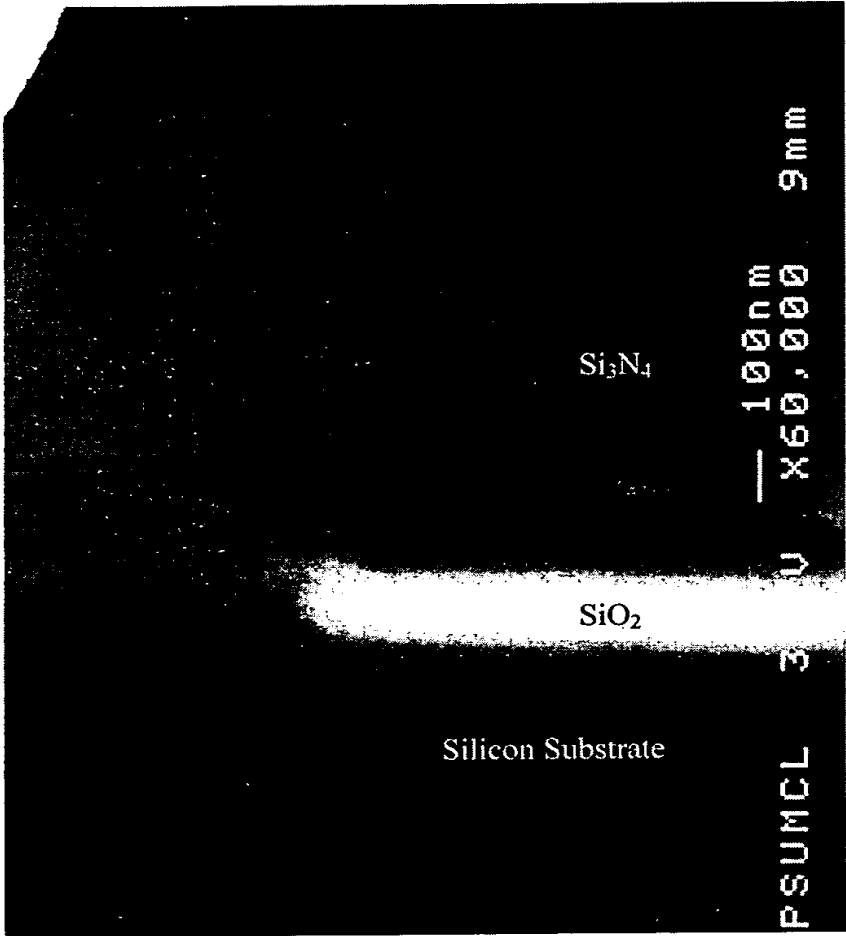
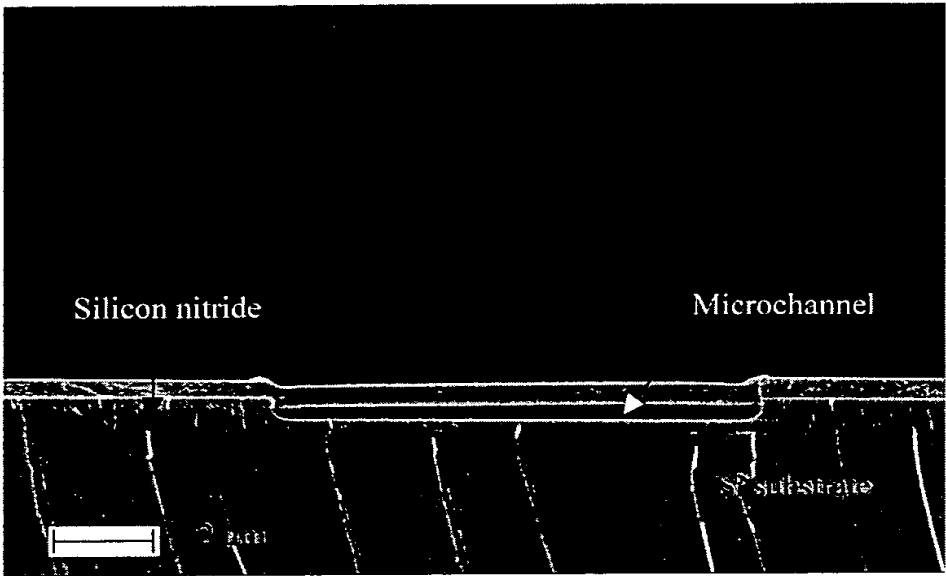


Figure 8

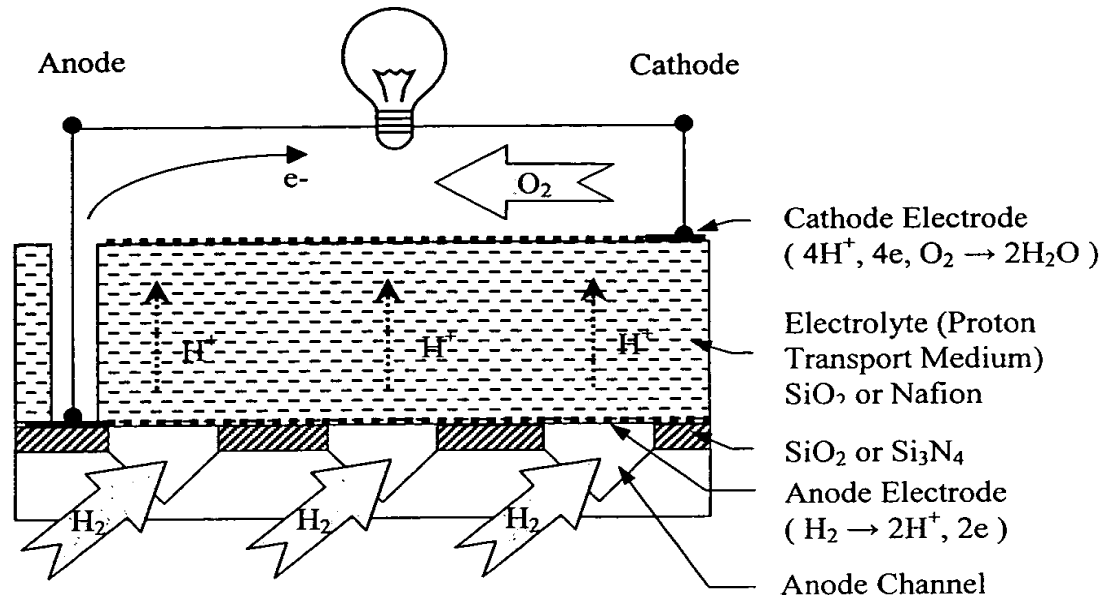


09030449 041701

Figure 9

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(a)



(b)

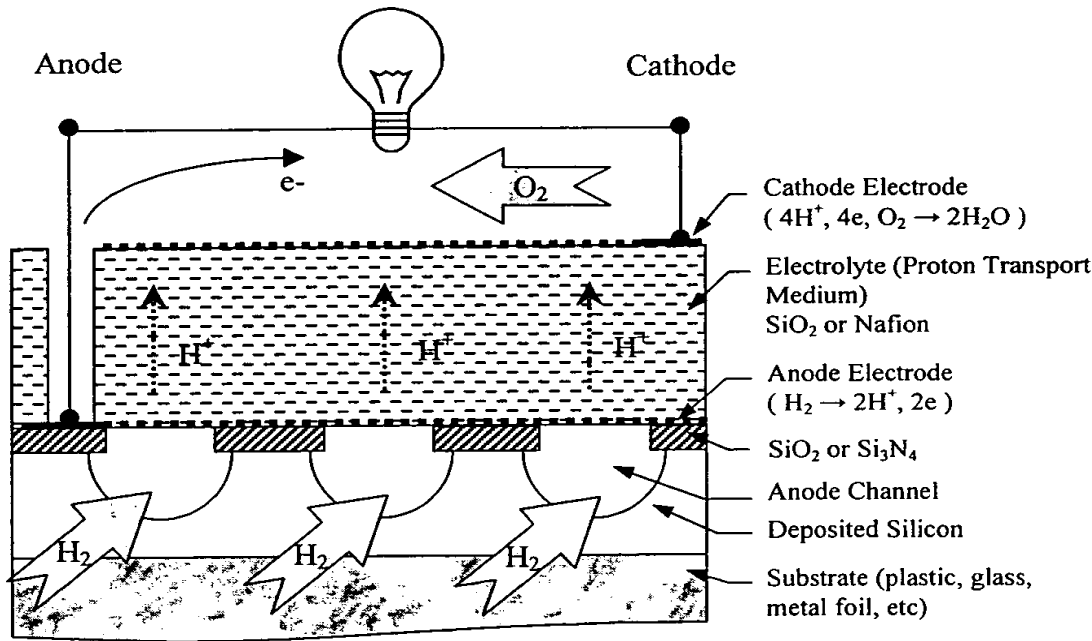
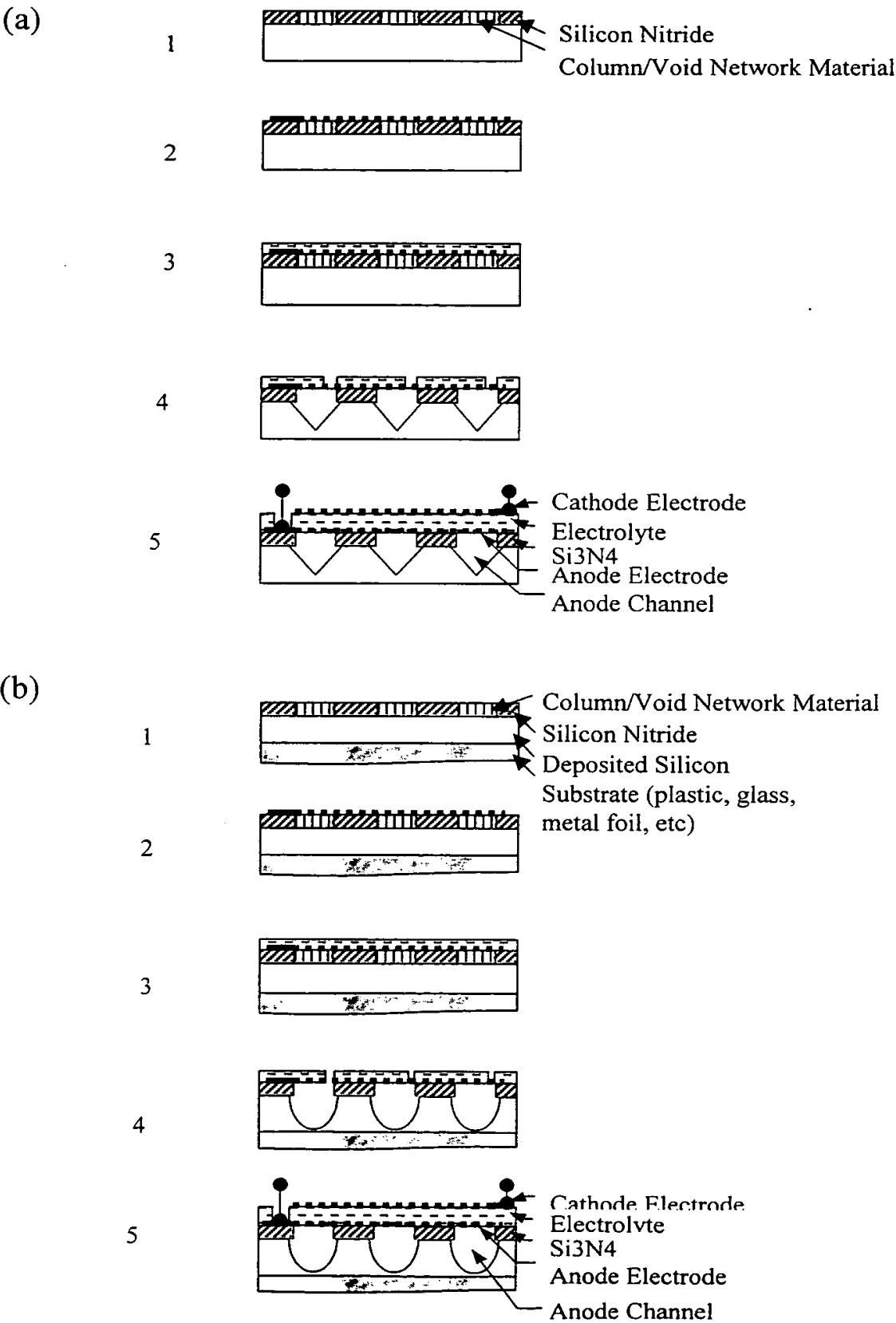


Figure 10



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[illegible]

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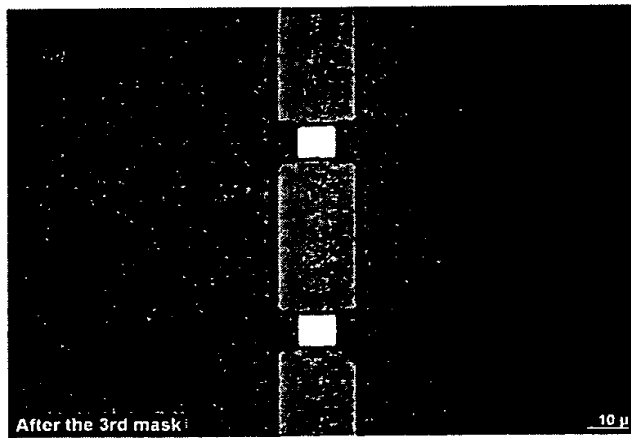
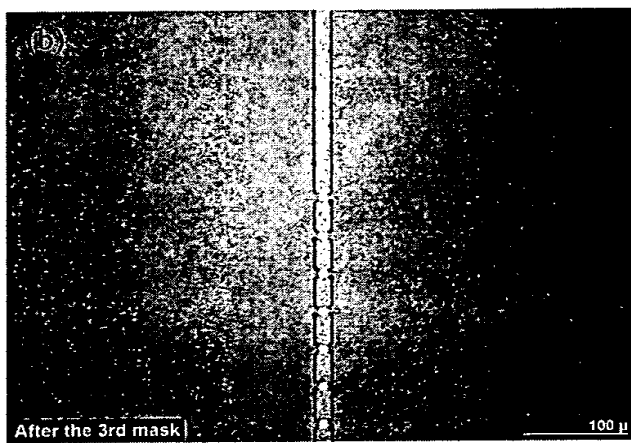
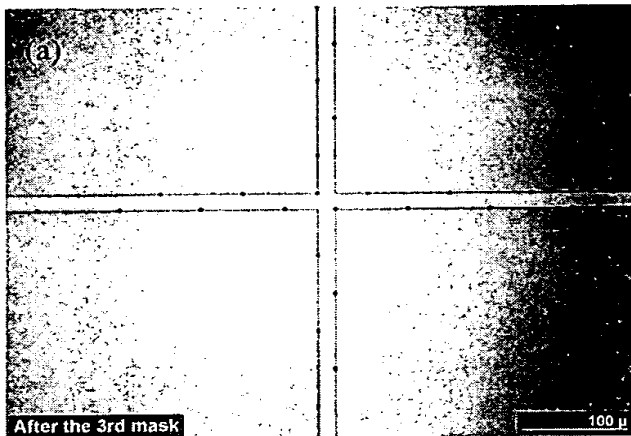


Figure 12

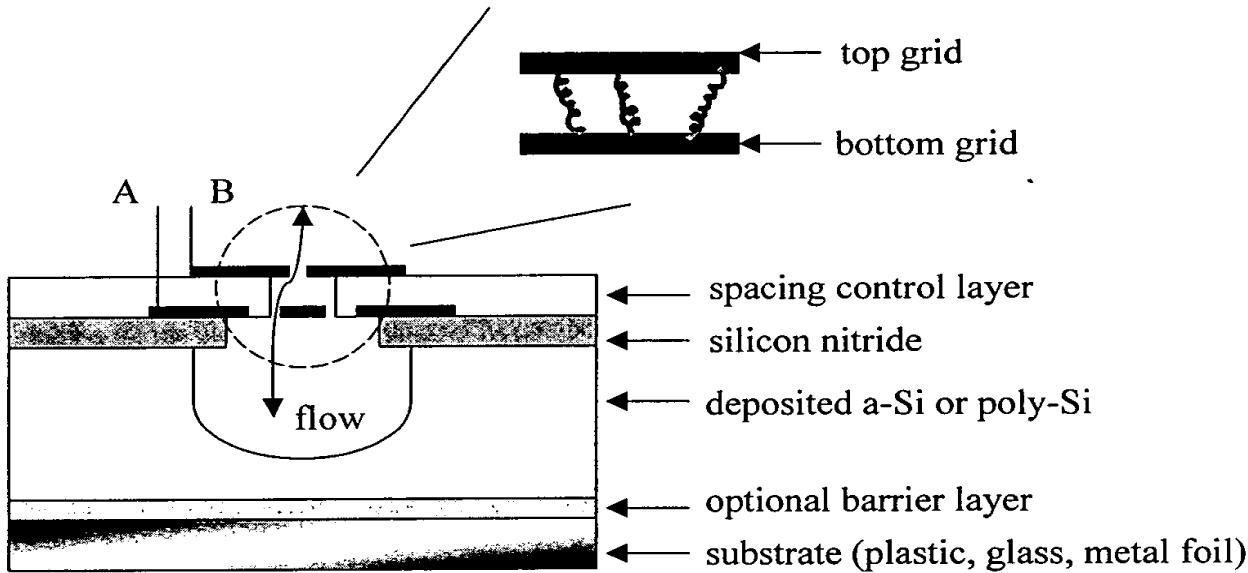


Figure 13

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(a) Cr/Au deposition



(b) Lithography and etching



(c) Column/void network material deposition



(d) Contact tip etching



(e) Beam support etching



(f) Lithography



(g) Au deposition



(h) Column/void network material etching

Figure 13: Cross-sectional diagrams of the device structure during fabrication.